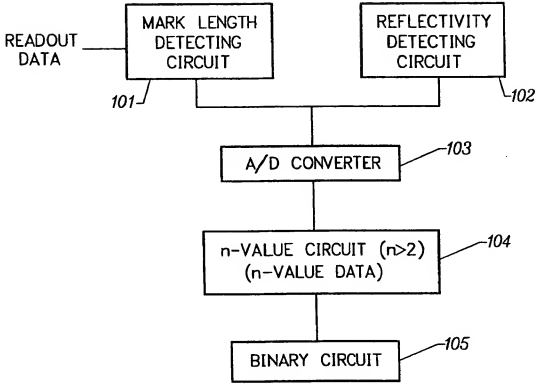


FIG. 1
(PRIOR ART)

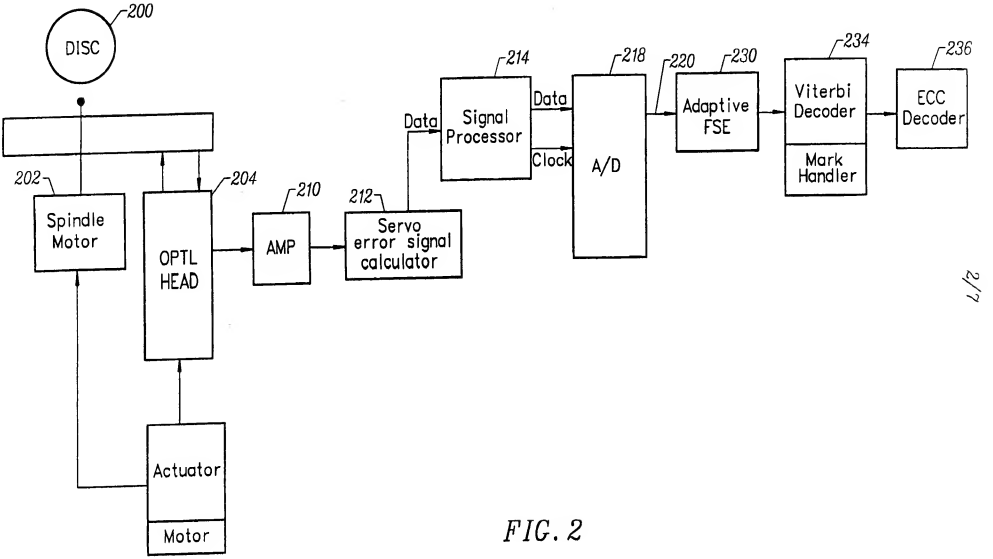

200
DISC
202
Spindle Motor
204
OPTL HEAD
210
AMP
212
Servo error signal calculator
Data
214
Signal Processor
Data
Clock
218
A/D
220
230
Adaptive FSE
234
Viterbi Decoder
Mark Handler
236
ECC Decoder
Actuator
Motor

FIG. 2

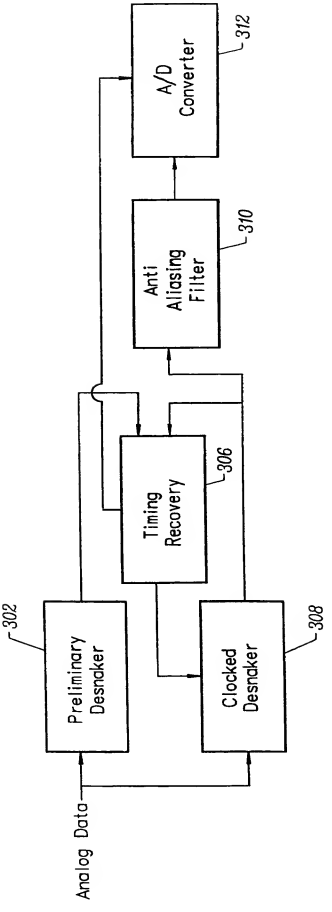

Analog Data
Preliminary Desnaker
302
Timing Recovery
306
Clocked Desnaker
308
Anti Aliasing Filter
310
A/D Converter
312

FIG. 3A

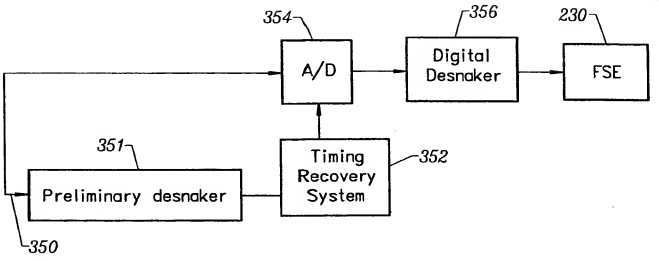

354
356
230
A/D
Digital
Desnaker
FSE
351
Timing
Recovery
System
352
Preliminary desnaker
350

FIG. 3B

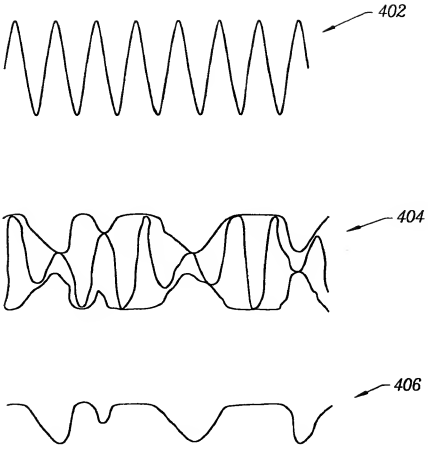


FIG. 4

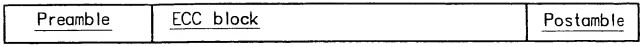


FIG. 5A

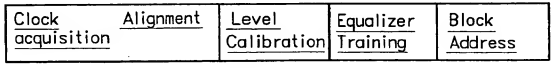


FIG. 5B

Preamble format

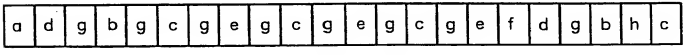
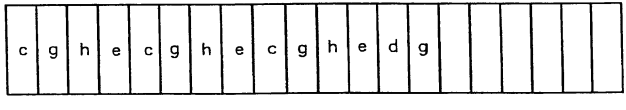


FIG. 5C

a address
b Erc data synch
c timing fields
d AGC
e DC
f ECC
g data
h trellis cleanup

Data block/ECC format

a d g b g c g e g c g e g c g e f d g b h c



c timing fields
g filler data
h trellis cleanup
e DC control
d AGC fields

Postamble format

c g h e c g h e c g h e d g

FIG. 5D

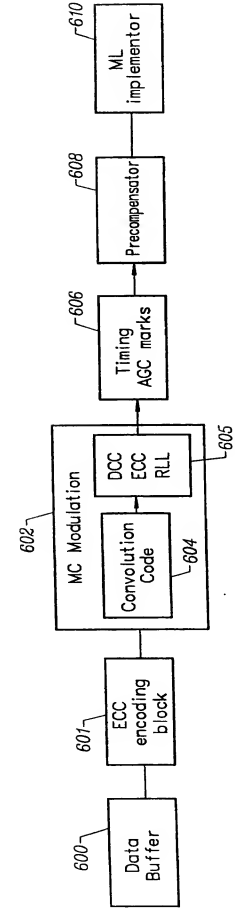

600
Data Buffer
601
ECC encoding block
602
MC Modulation
Convolution Code
604
DCC ECC RLL
605
606
Timing AGC marks
608
Precompensator
610
ML implementor

FIG. 6